Modeling of high-temperature superconducting pancake coils using the axisymmetric partial element equivalent circuit method

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Abstract—**The partial element equivalent circuit (PEEC) method has great potential to solve electromagnetic problems coupled with an electric circuit. Such capability is useful for modeling the integration of superconducting devices with power electronics converters. In this article we implement an axisymmetric PEEC model of pancake coils made of high-temperature superconducting (HTS) coated tapes fed by an arbitrary voltage source.**

Keywords*—*partial element equivalent circuit (PEEC), superconducting pancake coils.

I. INTRODUCTION

Superconducting devices are expected to operate into complex environments. For example, superconducting fault current limiters (ScFCL) have already been successfully integrated into high-voltage grids with voltages ratings going from 10.5 kV to 220 kV [1], [2]. In such environments, the superconducting device may interact with power transformers, transmission lines, circuit breakers, power electronic converters, and electric machines. Other examples of possible future integration of superconducting devices in complex environments can be found in the literature. In [3], the author proposes the integration of a superconducting power filter for HVDC grids, [4] presents the integration of such filter into an aircraft electric DC Grid and in [5] possible applications of ScFCLs in transmission and distribution systems are studied. From a modeling perspective, the main challenge is to model the superconducting device coupled to an electrical circuit.

The partial element equivalent circuit (PEEC) method [6] is an electric circuit oriented approach to model electromagnetic problems based on the integral form of Maxwell's equations. It is well suited to model devices within electrical circuits and it has been widely used for problems having a small number of degrees of freedom due to its good performance in computation time compared to finite element (FE) methods.

However, the disadvantages of the PEEC method start to appears for medium and large numerical problems since the circuit matrices are dense due to inductive and capacitive coupling [6]. Thus, using the classical PEEC rectangular cells [6] to model pancake coils would generate a rather large system of equations. To overcome this problem, we use the PEEC method with axisymmetric cells with rectangular cross-sections.

The article is organized as follows. In Section II, we derive the axisymmetric PEEC method and we explain its implementation for high-temperature superconducting pancake coils using an EJB constitutive law [7]. In Section III, we calculate current distribution and losses in AC and DC operation for an 8-turn HTS pancake coil and compare them with a FE model.

II. AXISYMETRIC PEEC

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III. SIMULATION RESULTS FOR AN 8-TURN PANCAKE COIL

We consider an 8-turn pancake coil wound with 1G powder-in-tube BSCCO tape of 4.5 mm width and 0.36 mm thickness. We model the BSCCO region and approximate it by a rectangular layer of 4.5 mm width and 45 μm thickness divided into 50 current cells. The central layer of BSSCO is coated on both sides by a rectangular silver layer of 4.5 mm width and 90 μm thickness followed by a rectangular copper layer of 4.5 mm width and 45 μm thickness, each one of these layers is modeled by a single current cell. The geometric parameters of the application are listed in Table I and its electrical parameters are listed in Table II.

The PEEC model of this arrangement leads to a 372-th order system of ODEs solved using the built-in ode23s solver of MATLAB. Here we assume that the HTS pancake coil is fed by an arbitrary voltage source $V_s(t)$.

To study current distribution on the HTS pancake coil in AC and DC, let us consider the coil to be fed by a DC voltage source $V_s(t) = 0.142$ and an AC voltage source

$V_s(t) = 0.47\cos(2\pi 50t)$. Both voltages sources will generate a peak current of 120 A (Fig. 1).

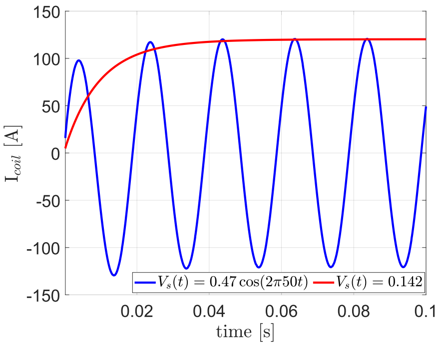

Fig. 1. Coil's current for voltage source excitation in AC and DC.

The resulting normalized current densities of the pancake coil in DC and AC are respectively plotted in Figs. 2 and 3. Notice that the space between layers is intentionally reduced for plotting.

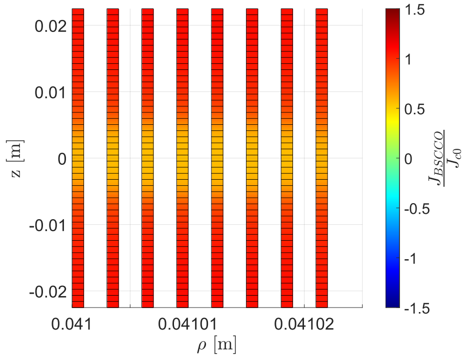

Fig. 2. BSSCO layer normalized current density for DC with 120 A peak at t = 0.0638 s.

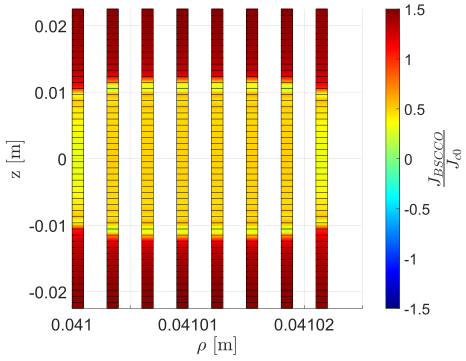

Fig. 3. BSSCO layer normalized current density for AC with 120 A peak at t = 0.0638 s (peak current of the 4-th period).

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TABLE I
SIMULATION PARAMETERS

Quantity	**Symbol**	**Value**
Tape width	w_t	4.5 mm
BSCCO layer thickness	th_{BSCCO}	45 μm
Silver layer thickness	th_{Ag}	90 μm
Copper layer thickness	th_{Cu}	45 μm
Coil length	L_{coil}	2 m
Coil internal radius	R_{in}	41 mm
Insulation thickness	th_i	0.18 mm

TABLE II
SIMULATION PARAMETERS

Quantity	**Symbol**	**Value**
Critical electric field	E_c	1×10^{-4} V/m
Power law exponent	n	13
Critical current density @ 77.3 K and self field	J_{c0}	2.148×10^{8} A/m^2
Constant for EJB law	B_0	0.0682 T
Constant for EJB law	k	0.0387
Constant for EJB law	α	1
Silver resistivity	ρ_{Ag}	1.59×10^{-8} Ω.m
Copper resistivity	ρ_{Cu}	1.72×10^{-8} Ω.m
Connector resistance	R_c	67.5 $\mu\Omega$

IV. CONCLUSION

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